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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,375	03/12/2004	Vijay K.G. Sindagi	TI-35832	7298

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EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,375	SINDAGI ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz Fleming
FRITZ FLEMING
Supervisory PRIMARY EXAMINER 4/14/2006
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on June 14, 2004. The papers filed have been placed on record.

Claim Objections

2. Claims 1-7 objected to because of the following informalities:

3. Examiner requests that "a plurality of functional units" on line 14 read "said plurality of functional units" because the limitation is written earlier in the claim (line 10). Further, Examiner requests that "a decode pipeline phase" on line 35 read "said instruction decode pipeline phase" because the limitation is written earlier in the claim (lines 6-7).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 (c) of this title before the invention thereof by the applicant for patent.

5. Claims 1, 2, 3, 4, 5, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kling (U.S. Patent No. 6,883,089 B2).

6. Regarding claim 1, Kling discloses a pipelined data processor capable of predicated instruction execution dependent upon the state of an instruction designated predicate register comprising: a data register file (Register File 168, see figs. 1A and 1B) including a plurality of read/write, general purpose data registers (see col. 3, lines 15 and 32); an instruction decode unit (Front end 160 and Register read 162)

Note that the term "decode unit" merely claims a device which decodes instructions. Therefore, the section of the processor which performs the register read and the front end in combination are considered to be a decode unit.

Operative during an instruction decode pipeline phase

Note that the definition of the word "phase" according to The American Heritage® Dictionary of the English Language, Fourth Edition is "An aspect; a part". Therefore, any phase in which the decode unit performs operations on an instruction is considered to be the instruction decode pipeline phase.

Receiving fetched instructions (see col. 3, lines 13-15) and determining the identity of at least one source operand data register (see col. 3, line 15), a destination operand data register (see col. 3, line 31-32) and one of a plurality of functional units for execution (see col. 2, lines 26-27 and 35-36) of each instruction, said instruction decode unit further identifying a predicate register (Scoreboard 170, see figs. 1A and 1B; col. 2, lines 46-50) responsive to receipt of a predicated instruction (see col. 3, lines 18-24); the plurality of functional units operative during an execution pipeline phase

Note that the definition of the word "phase" according to The American Heritage® Dictionary of the English Language, Fourth Edition is "An aspect; a part". Therefore, any phase in which the functional unit performs operations on an instruction is considered to be the instruction execution pipeline phase.

Connected to said instruction decode unit for performing a data processing operation (see col. 2, lines 26-29) on at least one source operand recalled from at least one corresponding instruction designated source data register (see col. 3, line 15) and producing a result (result; see col. 2, lines 52-55), said functional unit responsive to a predicate instruction (see col. 2, lines 54-55) to write said result to an instruction designated

Destination data register if said corresponding predicate data register has a first state (true) and to nullify said instruction (discarding the instruction) and not write said result if said predicate register has a second state opposite to said first state (false; see col. 3, lines 29-33); a scoreboard bit (if the operand is available) corresponding to each data register capable of serving as a predicate register (see col. 3, lines 16-21), each scoreboard bit connected to said instruction decode unit (see fig. 1A and 1B) to be set to a first digital state (not available) upon determining said corresponding data register is a destination for an instruction

Note that the operands are not available until the instruction is executed, therefore an indication must be set to show that the operand is not available. Since the processor checks this condition, it must be stored.

And connected to said plurality of functional units to be reset to a second digital state (available) opposite to said first digital state upon functional unit write of a result to said corresponding data register;

Note that the operands are not available until the instruction is executed, therefore an indication must be set to show that the operand is available when it is executed. Since the processor checks this condition, it must be stored.

And each functional unit is further operative responsive to a predicate instruction during the decode pipeline phase to nullify said predicate instruction (see col. 3, lines 9-12; col. 4, lines 31-45)

Note that the value of the predicate and scoreboard can be known in when the registers are read (decode phase; see above). Therefore, the instruction would be discarded in the decode phase.

Of a following execution phase (instruction that would have been executed in a following phase) if said predicate register has said second state and said corresponding scoreboard bit has said second state (see col. 3, lines 40-42).

7. Regarding claim 2, Kling discloses the pipelined data processor of claim 1, wherein: said functional unit is further operative to reset said scoreboard bit to said second digital state upon nullification of said instruction designating a corresponding data register as a destination operand data register.

Note that the processor must update the scoreboard in response to nullifying an instruction. If the scoreboard is not updated, the processor could stall indefinitely waiting for operands to become available.

8. Regarding claim 3, Kling discloses the pipelined data processor of claim 1, wherein: each functional unit is further operative to operate at a reduced power state for any execution pipeline phase nullified during said preceding instruction decode phase.

Note that when instructions are discarded, bubbles are sent through the processor. These bubbles generally take less power than instructions. Further, a reduced power state is a relative term. As such, the processor is always running at a reduced power state compared to something.

9. Claims 4-6 recite equivalent limitations as claims 1-3 respectively and are therefore anticipated by the method the processor of Kling uses (see above regarding claims 1-3).

10. Regarding claim 7, Kling discloses the method of claim 4 further comprising the step of: scheduling a last write to a data register a predetermined number of pipeline phases (1 phase)

Any amount of time can be considered one phase (see above regarding claim 1 about the interpretation of the word "phase").

Before an execution phase of a predicate instruction designating said data register as a predicate register (see col. 3, lines 9-12; col. 4, lines 31-45).

Note that instructions in an in-order processor are scheduled to be written to a register file in the writeback stage. A stall in the pipeline will change this schedule, but the instruction is scheduled to write results at a certain time. Further, the predicate instruction designating said data register as a predicate register must be following the instruction to write to that data register. Therefore, the last write to a data register must be scheduled before an execution phase of the predicate instruction.

Conclusion

11. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JM 4/10/06

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
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4/14/2006